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Novel Current-Scaling Current-Mirror Hydrogenated Amorphous Silicon Thin-Film Transistor Pixel Electrode Circuit with Cascade Capacitor for Active-Matrix Organic Light-Emitting Devices

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We proposed the hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) pixel electrode circuit with current-scaling function which is suitable for active-matrix organic light-emitting displays (AM-OLEDs). In contrast to the conventional current-mirror circuit, this circuit with the cascaded storage capacitors can provide a high data-to-organic light-emitting device (OLED) current ratio without increasing the a-Si:H TFT size. Moreover, since the number of signal line is reduced in the proposed pixel electrode circuit, the pixel electrode layout and the driving scheme can be simplified in comparison to previously reported cascade capacitor circuit. Finally, the proposed circuit can compensate for the threshold voltage variation of the driving TFT as well as the device geometric size mismatch and temperature effect. [DOI: 10.1143/JJAP.46.1343]

KEYWORDS: current driven, amorphous silicon (a-Si:H) TFT, pixel electrode circuit, current scaling, current mirror, AMOLED

1. Introduction

Over last several years, it was shown by several authors[1–3] that the current driving pixel electrode circuits are among the most desirable solutions for active-matrix organic light-emitting displays (AM-OLEDs). However, as display size and resolution increase, a large timing delay can be observed at a low data current and its importance increases with the display size.[4] To address this issue, several solutions have been proposed based on polycrystalline silicon (poly-Si) thin-film transistor (TFT) technology such as current-mirror circuit,[5,6] series-connected TFT circuit,[7] and current-mirror circuit with acceleration control line.[8] We also proposed hydrogenated amorphous silicon (a-Si:H) TFT based current-scaling pixel electrode circuit to address this problem.[4] In this paper, we present an improved a-Si:H TFT current driving pixel electrode circuit with a enhanced current scaling function. A current mirror circuit with a cascaded storage capacitor is proposed here to achieve a high data-to-organic light-emitting device (OLED) current ratio without increasing TFT size in comparison with the conventional current mirror pixel circuit. At the same time, by removing one control signal line, this circuit has a much simpler pixel circuit layout and driving scheme than the previous cascade capacitor pixel electrode circuit.

2. Operation of the Proposed Current-Scaling Pixel Electrode Circuit

The proposed current-driven pixel electrode circuit consists of two switching TFTs (T1 and T2), one mirror TFT (T4), one driving TFT (T3), and two storage capacitors (C_{ST1}, C_{ST2}) connected between a scan line and ground with a cascade structure, Fig. 1(a). The signals of V_{SCAN}, I_{DATA}, and V_{DD} are supplied by the external drivers while the anode of OLED is connected to V_{DD}. In comparison to the cascade capacitor current-scaling pixel electrode circuit reported previously,[4] by employing the current mirror TFT structure, the control signal line can be removed to simplify the pixel layout and driving scheme as well as to enable OLED to light up during ON-state even when top anode light-emitting device structure is used.

Here we define I_{OLED_ON} and I_{OLED_OFF} as the current flowing through OLED during the ON- and OFF-state, respectively. I_{OLED_OFF} is also defined as the scaled-down current from I_{OLED_ON} by the ratio of C_{ST2}/C_{ST1}. The pixel circuit operation mechanism can be described as follow: During the ON-state, V_{SCAN} turns on the T1 and T2, and I_{DATA} ($= I_{OLED\_ON}$) passes through T1 and T4 as the solid line shown in Fig. 1(a), and sets up the voltage at T2 drain electrode (node A). At the same time, I_{DATA} flows through T2 instantly enough to charge up the storage capacitor C_{ST1} and set-up the voltage at T4 gate electrode (node B) to allow I_{DATA} passing through T4. Since I_{DATA} is current source, the gate voltage of T4 is automatically set high enough to allow the fixed I_{DATA} flowing through T1 and T4. In the pixel circuit operation, different from the conventional current-mirror circuit, the current-scaling is not controlled by the geometry ratio of the transistors but by the ratio of capacitors, T3 and T4 are designed to have the same geometries ($W = 150\,\mu m$ and $L = 6\,\mu m$). The T1 size is set to be large enough ($W = 150\,\mu m$ and $L = 6\,\mu m$) to reduce the voltage drop over T1 when V_{SCAN} is on, while the T2 size is set to be small ($W = 10\,\mu m$ and $L = 6\,\mu m$) to reduce the voltage drop due to the parasitic capacitance when V_{SCAN} turns off. Since T3 and T4 are assumed identical in the ideal case and the gate bias (V_{B_ON}) is common to both TFTs, the same amount of current (I_{DATA}) is expected to flow through OLED to T3 by V_{DD}, which is expressed by,

$$I_{DATA} = \frac{1}{2}\mu_{FE} \cdot C_{OX} \cdot \frac{W_3}{L_3}(V_{GS} - V_{TH})^2 \qquad (1)$$

where μ_{FE} and C_{OX} are field-effect mobility and gate oxide capacitance of T3, respectively. The V_{B_ON} will be stored in both C_{ST1} and C_{ST2}, and the voltage across C_{ST2} is $V_{SCAN} - V_{B\_ON}$.

When the pixel changes from the ON- to the OFF-state, V_{SCAN} turns off T1 and T2. Because C_{ST2} is connected

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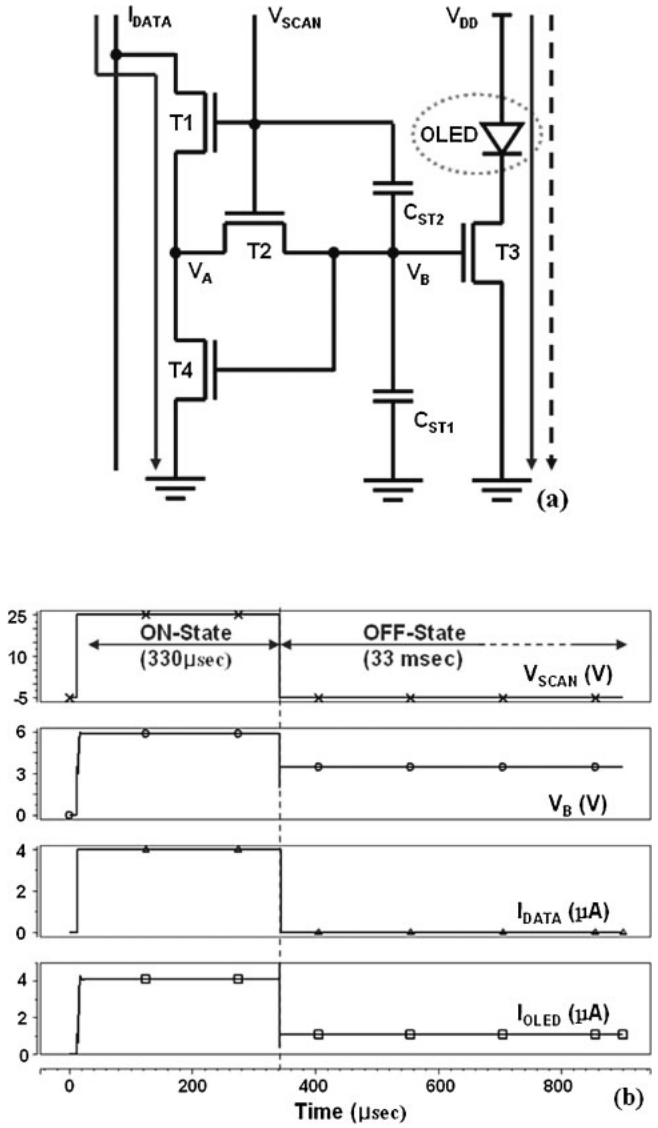


Fig. 1. Schematic of (a) the cascaded-capacitor current mirror pixel electrode circuit and (b) operational waveforms simulated by HSPICE.

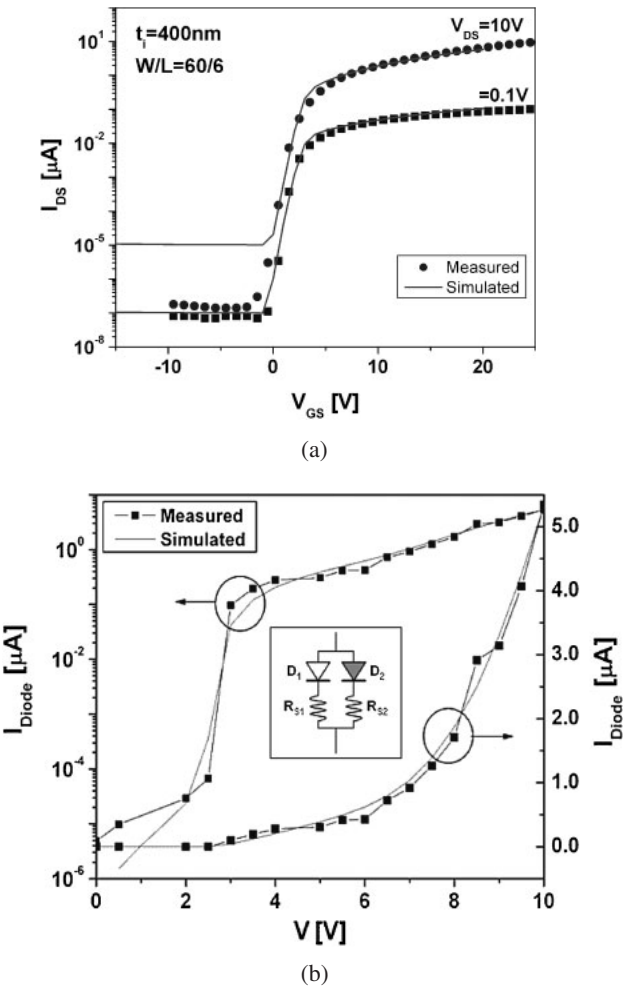


Fig. 2. Measured and simulated (a) transfer characteristics of a-Si:H TFT (b) current–voltage characteristics of white PLED. The equivalent circuit model of white PLED for simulation is shown in insert.

between the scan line and the node B to form a cascade structure with C_{ST1}, the change of V_{SCAN} will reduce V_{B_ON} to V_{B_OFF} due to the feed-through effect of the capacitors. V_{B_OFF} can be derived from the charge conservation theory[9] and is given by

$$V_{B\_OFF} = V_{B\_ON} - \Delta V_{SCAN} \times \frac{C_{ST2} \parallel C_{OV\_T2}}{C_{ST1} \parallel C_{OV\_T3} \parallel C_{OV\_T4} + C_{ST2} \parallel C_{OV\_T2}}, \quad (2)$$

where C_{OV_T2}, C_{OV_T3}, and C_{OV_T4} are the over-lapped capacitances between source-and-drain and gate of T2, T3, and T4, respectively. Their values used in the simulation are calculated as 50 fF, 0.75 pF, and 0.75 pF, respectively. If we assume that all over-lapped capacitances are negligible, eq. (2) can be simplified as

$$V_{B\_OFF} = V_{B\_ON} - \Delta V_{SCAN}\left(\frac{C_{ST2}}{C_{ST1} + C_{ST2}}\right).$$

A reduced T3 gate voltage (V_{B_OFF}) will be hold in C_{ST1} and C_{ST2} and it will continuously turn on T3 during the OFF-state. Since gate bias of T3 (V_{B_ON}) is reduced to V_{B_OFF} by the ratio of cascaded capacitor, a scaled-down data current (I_{OLED_OFF}) will flow through OLED, shown as the dashed line in Fig. 1(a). Consequently, when a very large data current (I_{DATA}) can be used to charge the pixel electrode to shorten the pixel programming time, a smaller driving current (I_{OLED_OFF}) can be achieved for lower gray scales at the same time.

3. Device Parameter Extraction

Synopsis H-SPICE simulation tool with the Rensselaer Polytechnic Institute (RPI) Troy, NY, a-Si:H TFT and diode models[10,11] were used to simulate the device characteristics and evaluate the proposed pixel electrode circuit. The a-Si:H TFT parameters developed within our group were used in this simulation,[3] and we measured the transfer characteristics of the fabricated a-Si:H TFT for different drain bias (0.1 and 10 V) by sweeping the gate bias from −10 to 25 V. Then, we simulated the measured transfer curves of a-Si:H TFT for each condition by H-SPICE.[12] The resulted transfer characteristics of a-Si:H TFT are shown in Fig. 2(a). To simulate the behavior of OLED, the conventional semiconductor diode model with the parameters extracted from organic polymer light-emitting diode (PLED) fabricated in our laboratory was used. The electrical property (current versus voltage) of PLED is shown in Fig. 2(b) and its opto-

Table I. Parameters used in pixel circuit simulation.

Device parameters of TFT	
W/L (T1, T3, T4) (μm)	150/6
W/L (T2) (μm)	10/6
C_{ST1} (fF)	360
C_{ST2} (fF)	30–90
ALPHASAT	0.5
EMU (eV)	0.02
EL (eV)	0.1
EPSI	6.9
KVT (V/°C)	−0.01
LAMBDA (1/V)	0.005
M	1.9
MUBAND [m^2/(V·s)]	0.00015
R_D (μΩ)	7000
R_S (μΩ)	7000
T_{OX} (m)	3×10^{-7}
V_{AA} (V)	500
V_O (V)	0.15
Device parameters of OLED	
n_1	18
n_2	2
R_{S1} (Ω)	7
R_{S2} (Ω)	150
I_{S1} (A)	10^{-8}
I_{S2} (A)	10^{-26}
Supplied signals	
V_{SCAN} (V)	−5/25
V_{DD} (V)	18
I_{DATA} (μA)	0.2–5

*Default values are used for other paramters which are not listed in the table.[10)]

electrical properties are described in our previous research.[13)] Since the opto-electrical behaviors of white PLED is different from the normal semiconductor diode, two semiconductor diode (D_1 and D_2) with series resistors (R_{S1} and R_{S2}) were used in parallel connection to fit the measured data of white PLED, and its equivalent circuit for the simulation is given in the insert. The a-Si:H TFTs and OLED parameters used for this pixel electrode circuit simulation are given in Table I.

4. Simulated Electrical Properties of the Proposed Pixel Electrode Circuit

The proposed current-scaling pixel electrode circuit was evaluated by H-SPICE and an example of waveforms is shown in Fig. 1(b). In this specific case, in ON-state, the voltage at node B is set to appropriate level to allow I_{DATA} of 1 μA to pass through T3 and T4 while V_{SCAN} and V_{DD} are hold at 25 and 18 V, respectively. The time for ON- and OFF-state was set to 0.33 and 33 ms, respectively. To investigate the current scaling ratio of the proposed pixel electrode circuit, we changed the I_{DATA} from 0.2 to 5 μA and measured the corresponding I_{OLED_ON} and I_{OLED_OFF} flowing through the diode for different ratios of cascaded-capacitors. In ON-state, the I_{OLED_ON} is identical to the data current (I_{DATA}), Fig. 3(a). When the pixel circuit operates in OFF-state, the diode current (I_{OLED_OFF}) is scaled-down by the ratio of cascade capacitor as discussed above and in our previous paper.[4)] From Fig. 3(b), it is obvious that the larger C_{ST2}/C_{ST1} results in significant decrease of the I_{OLED_OFF} at lower I_{DATA}. However, as shown in the figure, too large ratio of C_{ST2}/C_{ST1} ($> 1/6$) can result in the saturation of I_{OLED_OFF}, which eventually can deteriorate the current scaling function.

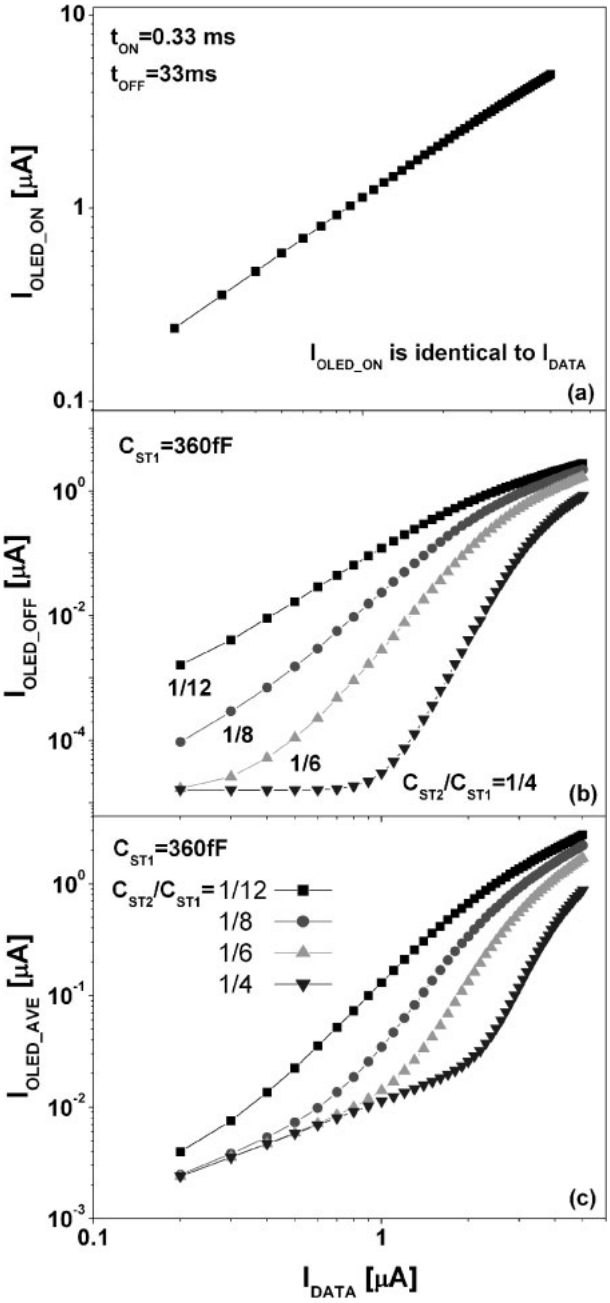
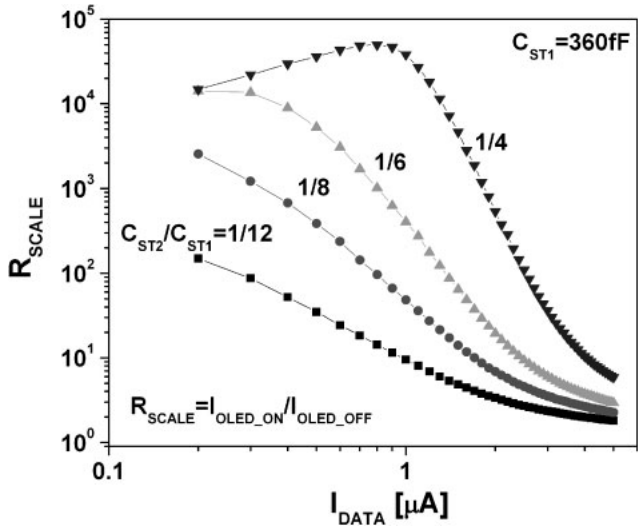


Fig. 3. Variation of the simulated I_{OLED_ON}, I_{OLED_OFF}, and I_{AVE} as a function of I_{DATA} for various C_{ST2}/C_{ST1} ratios.

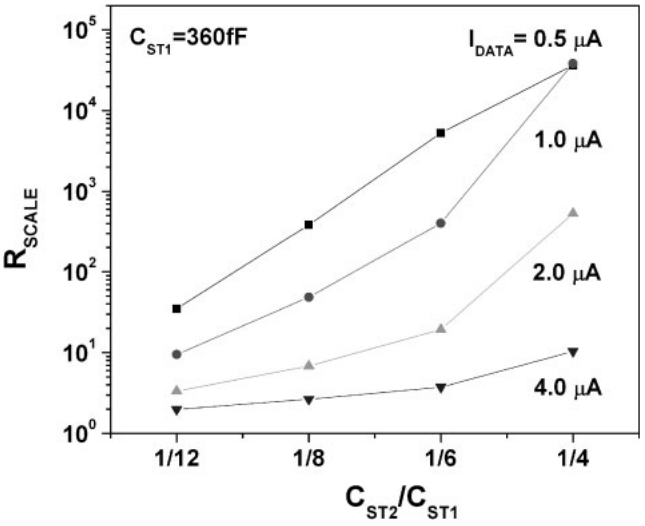
Since the OLED current value is different during ON- and OFF-state, we define the average OLED current (I_{AVE}) during one frame time,

$$I_{AVE} = \frac{I_{OLED\_ON} \cdot t_{ON} + I_{OLED\_OFF} \cdot t_{OFF}}{t_{ON} + t_{OFF}} \quad (3)$$

where t_{ON} and t_{OFF} is the ON- and OFF-period during the frame time, respectively. The variation of I_{AVE} versus I_{DATA} in one frame period ($t_{ON} + t_{OFF}$) for different C_{ST2}/C_{ST1}



(a)



(b)

Fig. 4. Variation of the current scaling ratio as a function of (a) I_{DATA} and (b) ratio of storage capacitances for the proposed pixel circuit.

ratios is shown in Fig. 3(c). Since the OFF-state period is much longer than ON-state, though I_{OLED_OFF} is very small during OFF-state, it can reduce the I_{AVE} even if the I_{OLED_ON} ($= I_{DATA}$) is large. For example, the pixel electrode circuit can generate I_{AVE} ranging from 2.4 nA to 2.1 μA while I_{DATA} swept from 0.2 to 5 μA. Therefore, during one frame time, we can achieve very wide range of OLED current levels by supplying high data current levels.

The evolution of the scaling ratio ($R_{SCALE} = I_{OLED\_ON}/I_{OLED\_OFF}$) for different ratios of C_{ST2}/C_{ST1} as a function of I_{DATA} is shown in Fig. 4(a). In this figure, we can see that for $C_{ST2}/C_{ST1} = 1/8$, R_{SCALE} decreases from 16190 to 2.35 as I_{DATA} increases from 0.2 to 5 μA, and an ideal non-linearity of R_{SCALE} can be achieved; e.g., a very high R_{SCALE} at low I_{DATA} levels (low gray scales) and a low R_{SCALE} at high I_{DATA} levels (high gray scales) can be produced. The variation of R_{SCALE} with the C_{ST2}/C_{ST1} is also shown in Fig. 4(b). The simulated results show that for fixed I_{DATA}, R_{SCALE} increases as C_{ST2} increase from 30 to 90 fF, corresponding to an increase of C_{ST2}/C_{ST1} from 1/12 to 1/4. For constant C_{ST2}/C_{ST1}, R_{SCALE} increases as I_{DATA} decreases as shown in Fig. 4(a). Therefore, for a fixed ratio of C_{ST2}/C_{ST1} determined from the pixel electrode circuit design, we can expect certain range of the output OLED current.

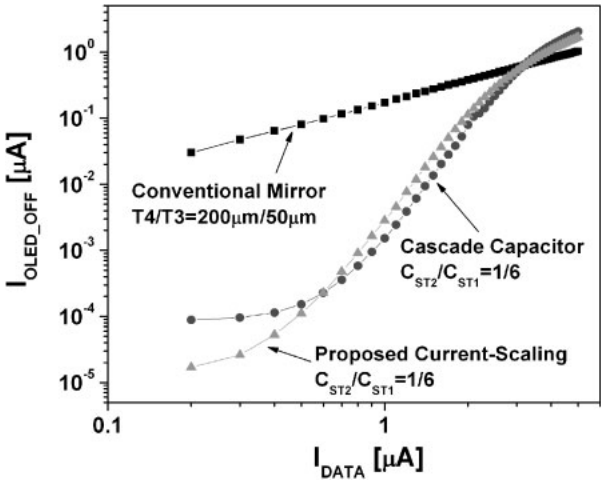


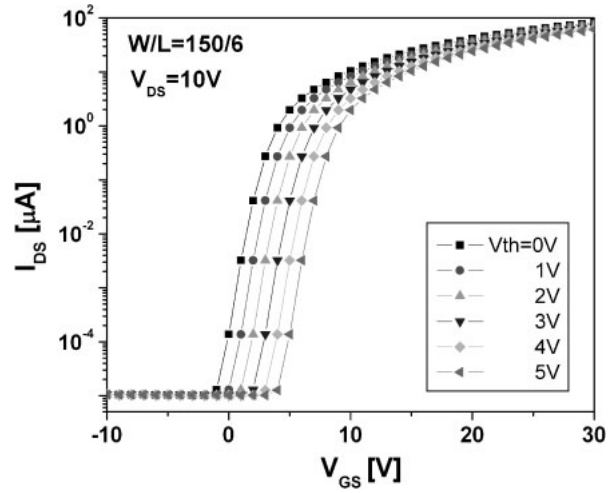
Fig. 5. Comparison of I_{OLED_OFF} vs I_{DATA} among conventional current-mirror, cascade-capacitor, and proposed pixel electrode circuits.

5. Comparison with Other Pixel Electrode Circuits

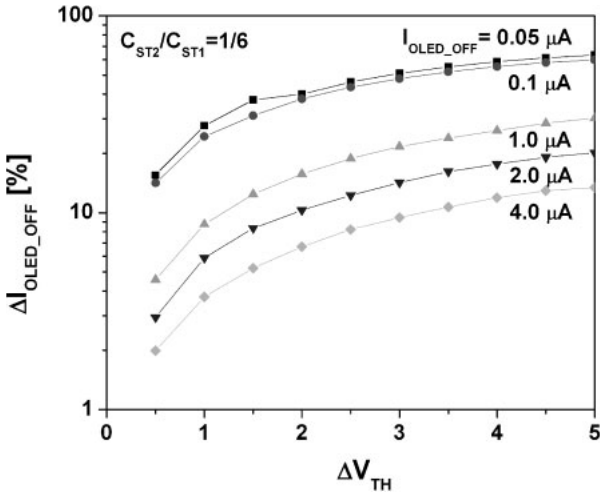
To demonstrate the current-scaling function of the pixel electrode circuit in comparison with both the conventional current-mirror[5] and cascade capacitor current-scaling pixel electrode circuits,[4] we simulated all three pixel electrode circuits using H-SPICE, and measured I_{OLED_OFF} as a function of I_{DATA} for each pixel electrode circuit as shown in Fig. 5. While the conventional current-mirror pixel circuit showed only a fixed current-scaling by the ratio of T4/T3 over given I_{DATA} range, the cascade capacitor current-scaling and the proposed current-scaling pixel electrode circuits showed non-linear current-scaling function for variable current-scaling ratio depending on I_{DATA}. When I_{DATA} varies from 0.2 to 5.0 μA, the proposed cascaded-capacitor pixel circuit with the ratio of $C_{ST2}/C_{ST1} = 1/8$ can provide I_{OLED_OFF} ranging from 1.7×10^{-5} to 1.7 μA. Hence much wider range of I_{OLED_OFF} levels can be achieved by this circuit in comparison with the conventional current-mirror pixel circuit (3.0×10^{-2} to 1.0 μA). And slightly wider range is obtained in comparison with the cascade capacitor current-scaling pixel circuit (8.8×10^{-5} to 2.0 μA).

6. Influence of Threshold Voltage Variation

To investigate the influence of the threshold voltage (V_{TH}) variation of T3 and T4 on pixel circuit performance, various threshold voltage deviations [$\Delta V_{TH} = V_{TH}$(after stress) − V_{TH}(initial)] have been used in pixel circuit simulation based on the experimental results reported previously.[3] In the H-SPICE a-Si:H TFT model, the threshold voltage is intentionally varied from 0 to 5 V, and it is applied to our a-Si:H TFT model to be used in the pixel circuit simulation. Figure 6(a) shows the change of transfer characteristics of a-Si:H TFT with the threshold voltage variation. In the proposed pixel circuit, since I_{OLED_ON} is not affected by the threshold voltage variation, the variation of I_{OLED_OFF} with



(a)



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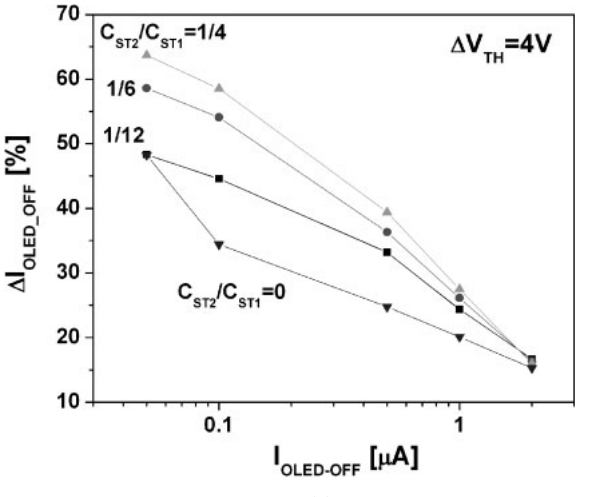


(c)

Fig. 6. (a) Changes of transfer curve at $V_{DS} = 30$ V, and (b) variation of ΔI_{OLED_OFF} as a function of TFT threshold voltage shift. (c) ΔI_{OLED_OFF} vs OLED current during display operation OFF-state for different C_{ST2}/C_{ST1} ratios when $\Delta V_{TH} = 4$ V.

ΔV_{TH} is used to estimate the influence of ΔV_{TH} on the performance of pixel circuit. For $C_{ST2}/C_{ST1} = 1/6$, the variation of the I_{OLED_OFF} with ΔV_{TH} can be defined by,

$$\Delta I_{OLED\_OFF} = \frac{I_{OLED\_OFF}(\Delta V_{TH}) - I_{OLED\_OFF}(\Delta V_{TH} = 0)}{I_{OLED\_OFF}(\Delta V_{TH} = 0)}. \quad (4)$$

The variation of I_{OLED_OFF} as a function of ΔV_{TH} is shown in Fig. 6(b). As ΔV_{TH} increases, ΔI_{OLED_OFF} also increases from around 4 to 25% when I_{OLED_OFF} is higher than 1.0 μA. In ideal case, I_{OLED_OFF} of T3 operation in deep saturation regime is independent of ΔV_{TH}. However, since the transconductance of T3 decreases with the increase of ΔV_{TH}, the drain voltage at T3 decreases as the ΔV_{TH} increases, resulting in the decrease of I_{OLED_OFF} caused by the channel length modulation effect.

Substantial increases of ΔI_{OLED_OFF} when I_{OLED_OFF} is lower than 100 nA is due to the influence of charge injection of switching T2 on V_{B_ON}. Since a small V_{B_ON} will result from a low driving current I_{DATA} at low gray scales, the charge carrier released from T2, when T2 is turned off, can reduce the V_{B_ON}. The variation of V_{B_ON} becomes large when the data current is small since the charge injection effect becomes larger at lower drain voltages. In other words, when the driving transistor (T3) operates just above the V_{TH} for expressing low gray scales, even small V_{TH} shift of TFT can lead to a large change of I_{OLED_OFF}. As shown in Fig. 6(c), when large C_{ST2}/C_{ST1} is used, a significant variation of ΔI_{OLED_OFF} at low gray scales is observed in comparison to $C_{ST2}/C_{ST1} = 0$. Therefore, smaller storage capacitor is needed to suppress the effect of T2 charge injection. From our data shown in Figs. 4(b) and 6(c), we can conclude that a large C_{ST2}/C_{ST1} can achieve a high R_{SCALE} but also result in a large ΔI_{OLED_OFF}.

7. Influence of Device Spatial Mismatch and Temperature

Mismatch of TFT geometric size and its operating temperature can also affect the stability of I_{OLED_OFF}. The TFT size mismatch usually can result from device fabrication processes such as over-etching and alignment errors. The heat generated by non-emissive recombination of electron and hole in OLED can also increase the substrate temperature leading to change of the electrical performance of TFTs. From eqs. (1) and (2), the OLED current in OFF-state can be given as

$$\begin{aligned} I_{OLED\_OFF} &= \beta(V_{GS} - V_{TH} - V_{offset})^2 \\ &= \beta\left(\sqrt{\frac{I_{OLED\_ON}}{\beta}} - V_{offset}\right)^2 \\ &= I_{OLED\_ON} - 2\sqrt{\beta \cdot I_{OLED\_ON}} \cdot V_{offset} \\ &\quad + \beta \cdot V_{offset}^2 \end{aligned} \quad (5)$$

where $\beta = \mu_{FE} C_{OX}(W_3/2L_3)$, $V_{offset} = \Delta V_{SCAN}(C_{ST2} \parallel C_{OV\text{-}T2}/(C_{ST1} \parallel C_{OV\text{-}T3} \parallel C_{OV\text{-}T4} + C_{ST2} \parallel C_{OV\text{-}T2}))$. It should be noted that I_{OLED_OFF} is sensitive to the spatial mismatch due to the V_{offset} in the second and third terms of eq. (5) while I_{OLED_ON} is less affected by this factor. Especially, since T3 and T4 are expected to be identical in the proposed circuit, TFT size mismatch can have critical influence on the pixel circuit performance. If we assume that the T3 width varies from the designed value ($W_3 = 150$ μm) while the T4 width is fixed, the variation of the I_{OLED_OFF} with the T3

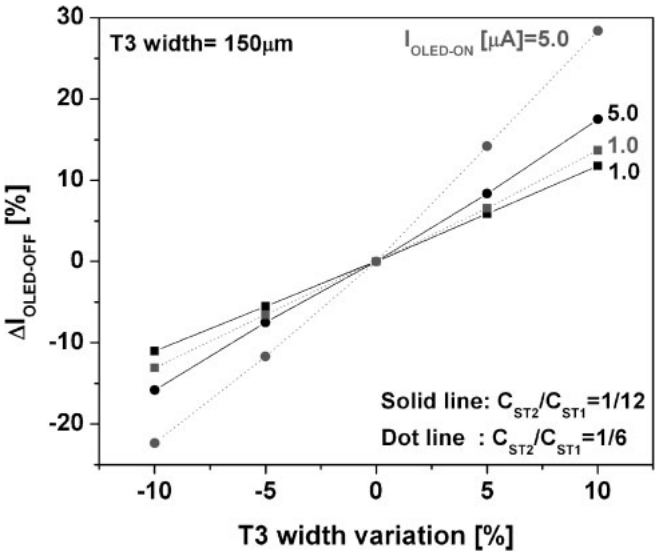


Fig. 7. Variation of I_{OLED_OFF} as a function of T3 width deviation.

width variation (ΔW_3) can be defined by eq. (6), and shown in Fig. 7.

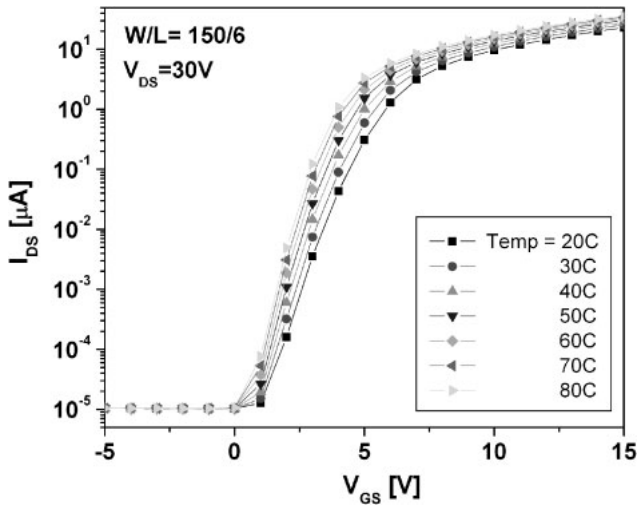
$$\Delta I_{OLED\_OFF} = \frac{I_{OLED\_OFF}(\Delta W_3) - I_{OLED\_OFF}(\Delta W_3 = 0)}{I_{OLED\_OFF}(\Delta W_3 = 0)} \quad (6)$$

The I_{OLED_OFF} changes by $\pm 25\%$ as the T3 width vary from 135 to 165 μm, corresponding to $\pm 10\%$ deviation. Also, according to eq. (5), a higher offset voltage value, associated with a large C_{ST2}/C_{ST1} ratio, will introduce greater deviation of I_{OLED_OFF}, Fig. 7. The ΔI_{OLED_OFF} for a high gray level is not as large as for a low gray level since a high driving current can reduce the sensitivity of I_{OLED_OFF} to the geometric size mismatch.

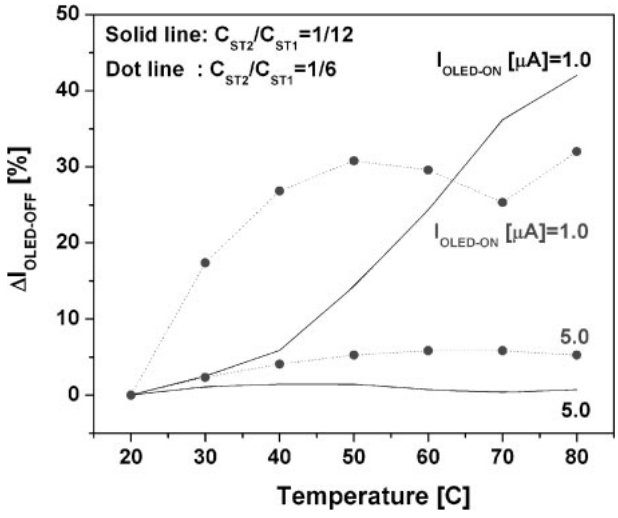
Since it is well known that the field-effect mobility μ_{FE} and threshold voltage V_{TH} in a-Si:H TFT can be influenced by device temperature,[14,15] the increasing temperature will result in higher field-effect mobility and lower threshold voltage thus giving a rise in ΔI_{OLED_OFF}. Figure 8(a) shows the simulated transfer curves of a-Si:H TFT at $V_{DS} = 30\,V$ when the temperature varies from 20 to 80 °C. As shown in the figure, as the temperature increase, the mobility also increases from 0.63 to 0.67 $cm^2/(V{\cdot}s)$ while the threshold voltage decreases from 2.84 to 0.32 V. The variation of the I_{OLED_OFF} with the temperature (T) can be defined by eq. (7), and shown in Fig. 8(b).

$$\Delta I_{OLED\_OFF} = \frac{I_{OLED\_OFF}(\Delta T) - I_{OLED\_OFF}(T = 20\,^{\circ}C)}{I_{OLED\_OFF}(T = 20\,^{\circ}C)} \quad (7)$$

A higher V_{offset} due to a larger C_{ST2}/C_{ST1} ratio can cause an increase of ΔI_{OLED_OFF} not only at a low gray level ($I_{OLED\_ON} = 1\,\mu A$) but also at a high gray level ($I_{OLED\_ON} = 5\,\mu A$) region. It should be mentioned that as the driving current increases, ΔI_{OLED_OFF} becomes smaller as a result of lower sensitivity to temperature achieved by a larger I_{OLED_ON}. Therefore, we can conclude that though the temperature and the device spatial mismatch have impact on the OLED current, the propose pixel circuit can compensate those deviations within acceptable operating error range (<30%).



(a)



(b)

Fig. 8. (a) Changes of transfer curve at $V_{DS} = 30\,V$ as a function of temperature. (b) Influence of operation temperature upon I_{OLED_OFF}.

8. Possible Application of the Proposed Pixel Electrode Circuit to AM-OLED

Figures 9(a) and 9(b) present schematic top views and cross-sections of proposed current-mirror with cascade capacitor pixel electrode circuit that can be used for a top-anode light emitting AM-OLED. The same sizes of TFTs and capacitors as used in the simulation were taken into consideration in the pixel electrode circuit layout. The pixel electrode circuit array layer can be fabricated by using the normal AM-LCD five-photomask process steps. Then, the planarization layer is deposited before the OLED fabrication. The cathode layer of OLED is made of aluminum (Al) or aluminum alloy coated with the metal thin layer such as magnesium (Mg) or calcium (Ca), and is deposited on top of planarization layer. Then electron-transporting layer (ETL), organic light-emissive layer (EL), and hole-transporting layer (HTL) are deposited successively over cathode electrode. Finally, transparent thin metal oxide (WO_3 or MoO_3)/ITO or Al bilayer is deposited as an anode to form a top-emission anode OLED structure.

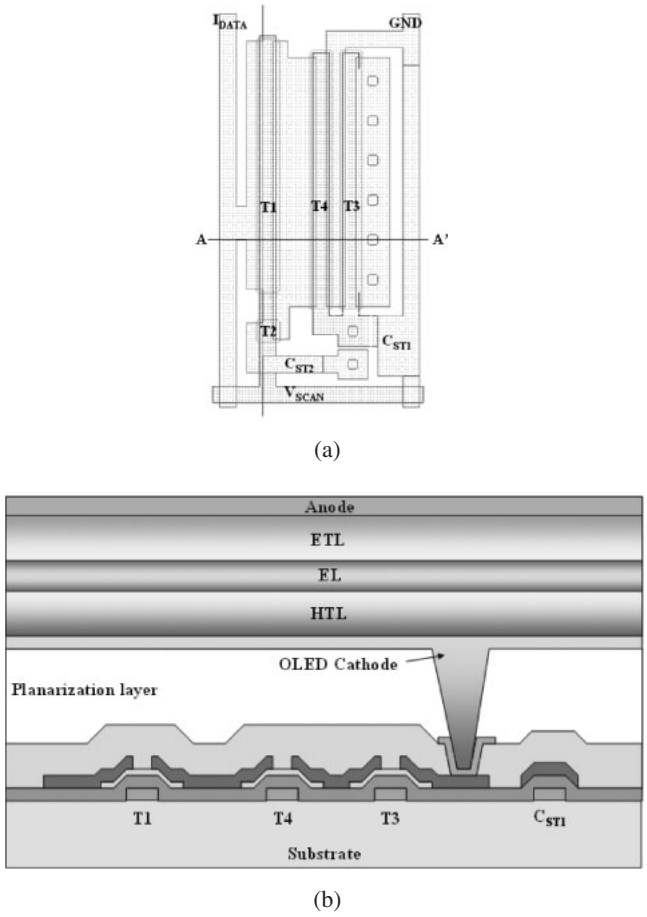


Fig. 9. (a) Schematic top views and (b) cross sections of proposed a-Si:H pixel electrode circuit.

9. Conclusions

When a low I_{DATA} is used to express a low gray scale, the conventional current-driven pixel circuit has a problem of slow programming time. On the contrary, when a high I_{DATA} is used to express a high gray scale, the current-mirror circuit has a problem of high power consumption due to a fixed current-scaling ratio. On the contrary, the cascade-capacitor circuit provides the comparable non-linear current-scaling to the proposed circuit but needs an additional control signal line which could complicate the pixel layout and driving scheme. In the proposed circuit, by employing the cascaded-capacitors connected to the driving TFT, we could produce better non-linear scaling-function than the cascade capacitor circuit, which has a high scaling ratio at low current levels and a low scaling ratio at high current levels. Furthermore, the threshold voltage variation of TFTs can also be compensated by the proposed circuit. The effects of device geometric size mismatch and temperature increase on pixel electrode circuit performance were analyzed. It has been concluded that the resulted deviations of the OLED current are within acceptable range for the operation ($< 30\%$). Therefore, using this pixel circuit, we expect to avoid the unnecessary pixel circuit power consumption at high current levels and minimize the programming time at low current levels with the reduced number of signal lines, which are supposed to be ideal characteristics for a high-resolution AM-OLED based on a-Si:H TFTs.

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